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B028313(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

(AICTE Scheme)

(Electronics & Telecommunication Engg. Branch)

DIGITAL SYSTEM DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Part (a) of all the questions is compulsory. Part (a) carries 4 maks. Attempt any* ***two*** *from from part (b), (c) and (d). Part (b), (c) and (d) carries 8 marks each.*

Unit-I

1. (a) Perform the following BCD addition : ~~8~~ 4

(i) 26 + 13

(ii) 579·6 + 636·8

(b) Prove the following Boolean expression : 8

(i) $A + A'B = A + B$

(ii) $AB + A'C + BC = AB + A'C$

(c) Reduce the expression

$$f = \Sigma\, m\,(1, 5, 6, 12, 13, 14) + d\,(2, 4)$$

and implement the real minimal expression using universal logic. 8

(d) Realize the XOR function using :

(i) AOI Logic,

(ii) NAND Logic, and

(iii) NOR Logic 8

Unit-II

2. (a) Design Full Adder using two Half Adders. 4

(b) Design a 4-line-to-16-line Decoder using 3-line-to-8-line Decoder. 8

(c) Implement the following logic function using an 8XI MUX

$$F\,(A, B, C, D) = AB' + BD + B'CD'$$ 8

(d) Design 4-bit BCD Adder and draw its logic diagram. 8

Unit-III

3. (a) What is meant by race around condition in flip flops and how this problem can be eliminated? 4

(b) Convert J-K flip flop to S-R Flip flow. 8

(c) Design a 4-bit universal shift register and draw the logic circuit diagram. 8

(d) Design a Synchronous BCD Counter using J-K Flip flops. 8

Unit-IV

4. (a) Define Mealy model and Moore model. 4

(b) What is a serial adder? Explain its working with the help of a state diagram and a state table. 8

(c) Draw and explain the ASM chart for sequence detector. 8

(d) Design 3-bit odd parity generator with the help of a state diagram and a state table. 8

Unit-V

5. (a) Compare the logic families in terms of commonly used specification parameters. 4

(b) With the help of a neat diagram, explain the working of IIL NAND and NOR Gates. 8

(c) With the help of a neat diagram, explain the working of a two-input TTL NAND gate with Totem-pole output. 8

(d) With the help of a neat diagram, explain the working of a two-input ECL OR/NOR gate. 8